II. REMARKS

Claims 1-38 are pending. The Applicants' attorney has amended claims 1, 11, 14-15, 20-24, 26-28, 31, 34-36, and has added new claim 38; but these amendments and new claim add no new matter to the patent application. In light of the following, all of the claims as amended are now in condition for allowance, and, therefore, the Applicants' attorney requests the Examiner to withdraw all of the outstanding rejections. But if after considering this response the Examiner does not allow all the claims, the Applicant's attorney requests that the Examiner contact him to schedule a teleconference to further the prosecution of the application.

Amendments to the Specification

The Applicants' attorney has amended the specification to correct typographical errors. But these amendments add no new matter to the patent application.

Objection to the Drawings

The Applicants' attorney has amended the drawings per the enclosed Request for Drawing Change to overcome this rejection and to correct other minor errors. But these amendments add no new matter to the patent application.

Rejection of Claims 27-33 Under 35 U.S.C. § 112 Second Paragraph

In claim 27, the Applicants' attorney has amended "the second address" in line 4 to "the first address" to overcome this rejection. But this amendment merely corrects a typographical error, and does not narrow the scope of the claims.

Rejection of Claims 1-17 and 20-37 Under 35 U.S.C. § 102(e) as Being Anticipated By U.S. Patent Application 2002/0110037 to Fukuyama et al.

As discussed below, the Applicants' attorney disagrees with this rejection.

Claim 1

Claim 1 as amended recites a memory comprising an address bus operable to receive an external address, an address counter operable to generate an internal

address, a comparator coupled to the address bus and operable to compare the external address to a value, and a control circuit coupled to the comparator and operable to terminate a data-transfer cycle based on the relationship between the external address and the value.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a memory 26 includes a column address bus (*e.g,* the output of the column address buffer 44) that receives an external column address from a processor 64 (FIG. 6) or other source external to the memory 26, a column-address anticipation counter 14 operable to generate an internal column address, and a comparator 18 operable to compare the external column address to a value. A control circuit 24 terminates a read or a write cycle based on the relationship between the external address and the value. Examples of this value include the interal column address from the counter 14 and the contents of the page-length register/counter 16. For example, per the timing diagram of FIG. 3, the control circuit 24 terminates a read cycle when the external address does not equal the internal address, and enables the read cycle when the external address equals the internal address.

In contrast, Fukuyama does not disclose comparing an external address to a value and terminating a data-transfer cycle based on the relationship between the external address and the value. Referring, *e.g.*, to FIG. 7 and paragraph [0050] of Fukuyama, the comparators 24 and 25 compare an input (external) row/bank address from the decoder 21 with an access row/bank address (value) and a next-access row/bank address (value) respectively. In response to these comparisons, a generator 44 determines whether the location addressed by the input row/bank address has been pre-activated. If the addressed location has been preactivated, then the generator 44 enables a generator 43 to issue read/write commands that allow a read/write from/to the addressed location; if the addressed location has not been preactivated, then the generator 44 activates the addressed location and disables the generator 43 from issuing read/write commands until the addressed location is activated. But this activation-and-disable step is merely part of the read/write cycle, with the disable being a mere delay within the read/write cycle until the address location is activated. Consequently, unlike the claimed control circuit, Fukuyama's generator 44 does not terminate a data-transfer cycle.

Furthermore, Fukuyama's generator 44 does not terminate a data-transfer cycle in response to the burst comparator 45 (*see, e.g.,* paragraphs [0119] – [0122]).

Claim 20

Claim 20 as amended recites a memory circuit including an address counter operable to generate an internal address during a data–transfer cycle, a storage circuit operable to receive and store a value before or during the data-transfer cycle, and a control circuit coupled to the storage circuit and operable to terminate the data–transfer cycle in response to the stored value.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a memory 26 includes a column-address anticipation counter 14 for generating an internal column address, a page-length register/counter 16 (storage circuit) for receiving and storing a value, and a control circuit 24 for terminating a read or a write cycle in response to the value stored in the register/counter 16. For example, the register/counter 16 may store an ending address, and, per the timing diagram of FIG. 3, the control circuit 24 terminates a read cycle when the external address or internal address equals the stored ending address, and enables the read cycle when the external address or internal address does not equal the stored ending address.

In contrast, Fukuyama does not disclose terminating a data-transfer cycle in response to a stored value. Referring, *e.g.*, to FIG. 7 and paragraph [0050] of Fukuyama, the comparators 24 and 25 compare an input (external) row/bank address from the decoder 21 with an access row/bank address (stored value) and a next-access row/bank address (stored value) respectively. In response to these comparisons, a generator 44 determines whether the location addressed by the input row/bank address has been pre-activated. If the addressed location has been preactivated, then the generator 44 enables a generator 43 to issue read/write commands that allow a read/write from/to the addressed location; if the addressed location has not been preactivated, then the generator 44 activates the addressed location and disables the generator 43 from issuing read/write commands until the addressed location is activated. But this activation-and-disable step is merely part of the read/write cycle, with the disable being a mere delay within the read/write cycle

until the address location is activated. Consequently, unlike the claimed control circuit, Fukuyama's generator 44 does not terminate a data-transfer cycle.

Claim 23

Claim 23 as amended recites a method comprising comparing a received address to a generated address and terminating a cycle during which data is being transferred to or from a storage location residing at the generated address if the received address does not have a predetermined relationship to the generated address.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a comparator 18 compares a received external column address with an internal column address generated by a counter 14, and a column decoder 38 transfers data to/from a location of the array 30 residing at the internal column address. A control circuit 24 terminates this data-transfer cycle if the external column address does not have a predtermined relationship to the internal column address. For example, per the timing diagram of FIG. 3, the control circuit 24 may terminate the data-transfer cycle if the internal column address does not equal the external column address.

In contrast, Fukuyama does not disclose comparing a received address to a generated address and terminating a data-transfer cycle if the received address does not have a predetermined relationship to the generated address. Referring, *e.g.*, to FIG. 7 and paragraph [0050] of Fukuyama, none of the comparators 24, 25, and 45 compare the external address from the address decoder 21 to the internal address generated by the address counter 42. Furthermore, as discussed above in support of the patentability of claims 1 and 20, Fukuyama's generator 44 does terminate a data-transfer cycle.

Claim 27

Claim 27 as amended recites a method comprising generating a first address, comparing the first address to a predetermined value, and terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a column-address anticipation counter 14 generates an internal column (first) address and data is transferred to or from the location in the array 30 at the internal column address. A comparator 18 compares the internal column address to a predetermined value stored in the register/counter 16, and the control circuit 24 terminates the data-transfer cycle if the internal column address has a predetermined relationship (*e.g.*, is equal) to the value stored in the register/counter 16.

In contrast, Fukuyama does not disclose comparing a generated address to a predetermined value and terminating a data-transfer cycle if the generated address does not have a predetermined relationship to the predetermined value. Referring, *e.g.*, to FIG. 7 and paragraphs [0119] – [0122] of Fukuyama, although the comparator 45 compares a generated address from the address counter 42 to a predetermined value, the generator 44 does not terminate a data-transfer cycle in response to this comparison (signal 52).

Claim 34

Claim 34 as amended recites a method comprising loading a memory with a count value from an external source, generating a first address inside of the memory, the first address being distinct from the count value, incrementing or decrementing the count value, comparing the count value to a predetermined value, and terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the count value has a predetermined relationship to the predetermined value.

For example, referring to FIGS. 3-6 and pages 6-11 of the patent application, a register/counter 16 is loaded with a count value from an external source such as a processor 64, a column-address anticipation counter 14 generates an internal column (first) address that is distinct from the count value in the register/counter 16, the register/counter 16 increments or decrements the count value, the comparator 18 or the control circuit 24 compares the count value to a predetermined value, and the control circuit 24 terminates the data-transfer cycle during which data is

transferred to or from the location(s) in the array 30 at the internal column address(es) if the count value equals the predetermined value.

In contrast, Fukuyama does not load a count value from an external source and generate an address that is distinct from the count value, does not increment or decrement the count value, and does not terminate a cycle during which data is being transferred to or from a storage location residing at the address if the count value has a predetermined relationship to a predetermined value. Referring, *e.g.*, to FIG. 7, Fukuyama's address counter 42 generates an address, but nowhere does Fukuyama load from an external source a count value that is distinct from the address generated by the counter 42. Consequently, Fukuyama cannot increment/decrement such a count value, or terminate a data-transfer cycle in response to such a count value.

Rejection of Claims 18-19 Under 35 U.S.C. § 103(a) as Being Unpatentable Over Fukuyama In View Of U.S. Patent 6,484,231 to Kim

As discussed below, the Applicants' attorney disagrees with this rejection.

Claim 18

Claim 18 as amended recites a a memory circuit including an address bus operable to receive an external address, an address counter operable to generate an internal address, an address decoder, and a multiplexer coupled to the address bus, the address counter, and the address decoder and operable to couple either the external address or the internal address to the address decoder.

For example, referring to FIGS. 4-5 of the patent application, a memory circuit 26 includes an address bus (input of column address buffer 44) for receiving an external column address, an address counter 14 for generating an internal column address, a column-address decoder 38, and a multiplexer 22 for coupling either the external column address or the internal column address to the column-address decoder 38.

In contrast, the combination of Fukuyama and Kim does not suggest a multiplexer operable to couple either an external address or internal address to an address decoder. Referring, *e.g.*, to Fukuyama's FIG. 7, Fukuyama does not

disclose a multiplexer. Referring to Kim's FIG. 4, although Kim discloses a multiplexer 100, this multiplexer does not couple any address to the address decoder 50, but instead couples data to/from a selected cell block 61-64 from/to data I/O pads 9 via respective sense amplifiers 71-74 to speed up the writing and reading of data. Therefore, the combination of Fukuyama and Kim would at most suggest incorporating Kim's data I/O multiplexer 100 between Fukuyama's I/O pads and sense amplifiers (neither shown in Fukuyama), and would not suggest adding to Fukuyama's circuit a multiplexer that couples either the external address (input to the address decoder 21) or the internal address from the address counter 42 to the address decoder 21.

Conclusion

In light of the foregoing, claims 2-10, 12-13, 16-19, 25, 29-30, and 32-33 as previously pending, claims 1, 11, 14-15, 20-24, 26-28, 31, and 34-36 as amended, and new claim 38 are in condition for full allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 12th day of July, 2004.

Respectfully Submitted,

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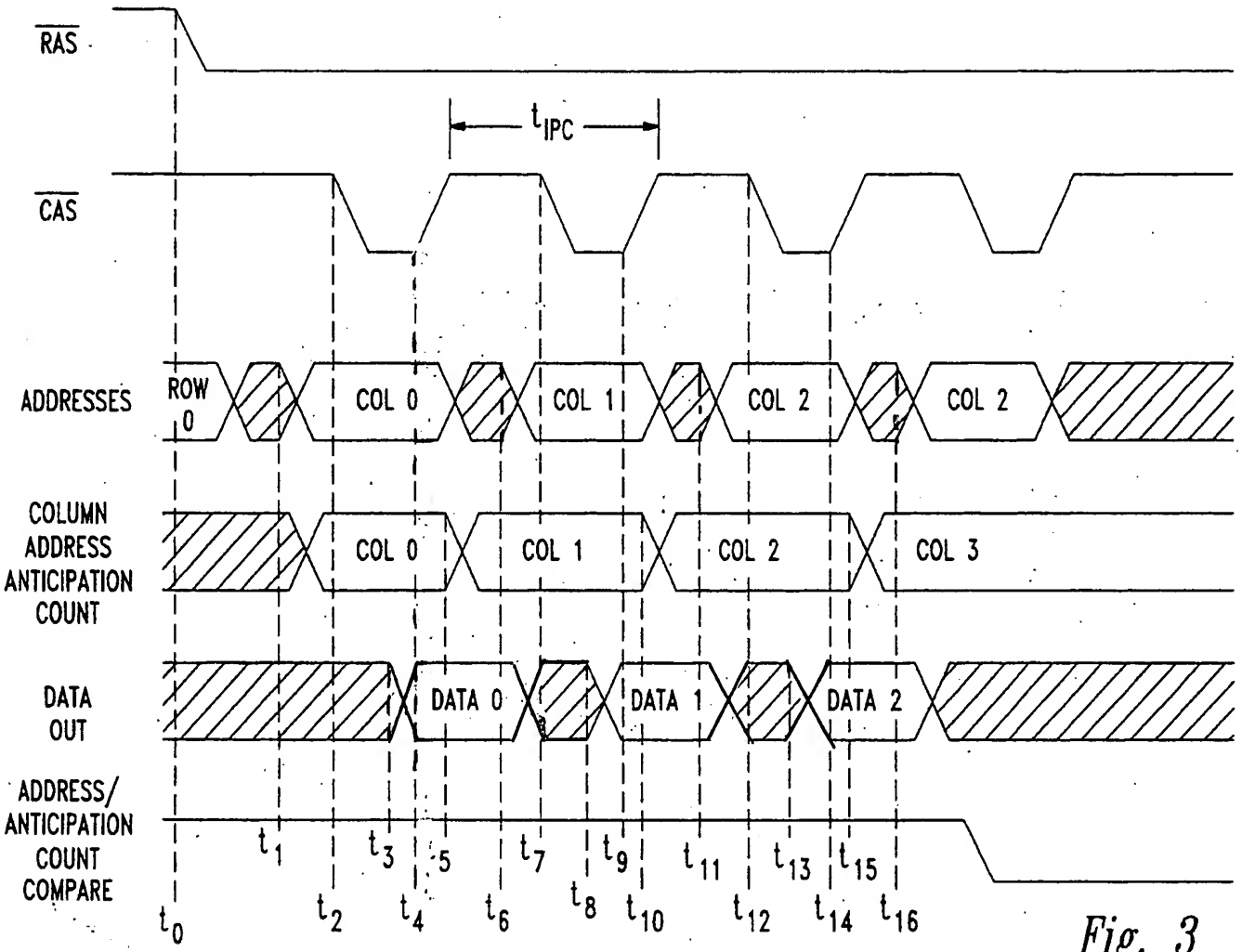

Fig. 3

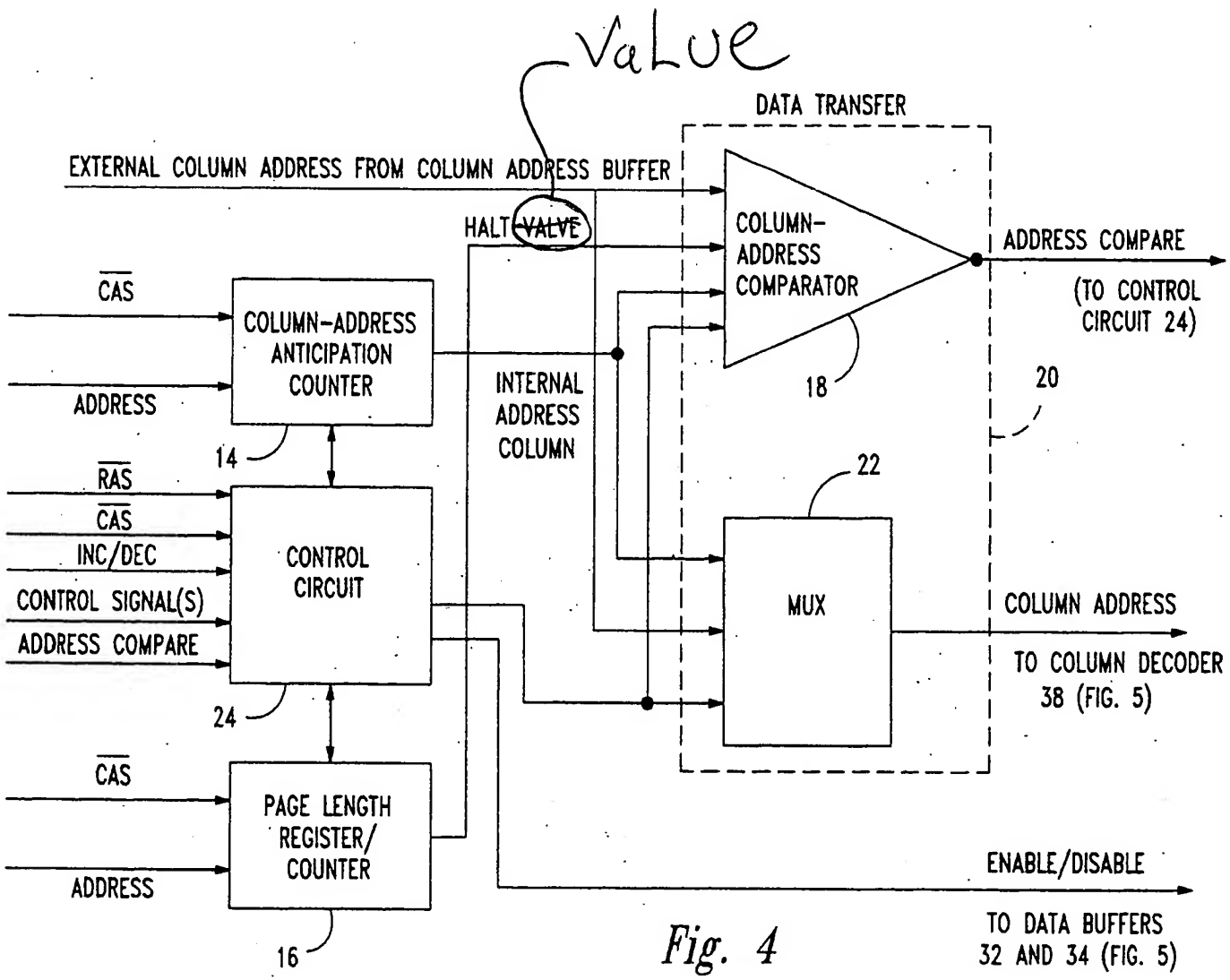

Fig. 4